Chapter 6

PDA Hardware Module GP1

Original, 08/96

CONTENTS – PDA unit

Page No

List of Figures

[This page intentionally left blank]

Introduction

This chapter describes the PDA system hardware used in the NOKIA 9000 communicator. The PDA module is used to run all applications that utilise the bigger (640x200) LCD screen.

Technical Summary

Table 1. List of functional blocks on PDA module

Name of functional block	Function
PROCU	Execution and interface unit for PDA
PDAPWRU	Power supply unit
SIRU	Serial communication and Infrared Unit
EMIU	EMI supressing Unit

Most of the engine functionality is integrated on a chip that combines a CPU core and all needed peripherals; this chip and all other PDA module circuitry are mounted on a single multilayer printed circuit board. The chassis of the NOKIA 9000 communicator separates the CMT and PDA modules and also protects PDA circuits from EMI.

The components of the PDA system hardware are surface mounted soldered using reflow. The bottom connector (system connector) carries two optional through hole pins which might prove useful i.e., soldered by hand, if so required.

All PDA module components are located to one side of the PCB; the other side of the PCB is used for QWERTY keypad wiring matrix. The connection to the CMT module is made using a board to board connector and the connections from CMT to the phone User Interface module (UIF) are made through the PDA module. The connections to the PDALCD module and phone user interface module excluding audio, SIM card holder, buzzer, and call LED (UIF) are made using a flex cable.

The CMT module controls the battery charging via system connector on PDA. Test pads located to the PCB under the battery pack are for CMT flash loading and fieldtest purposes.

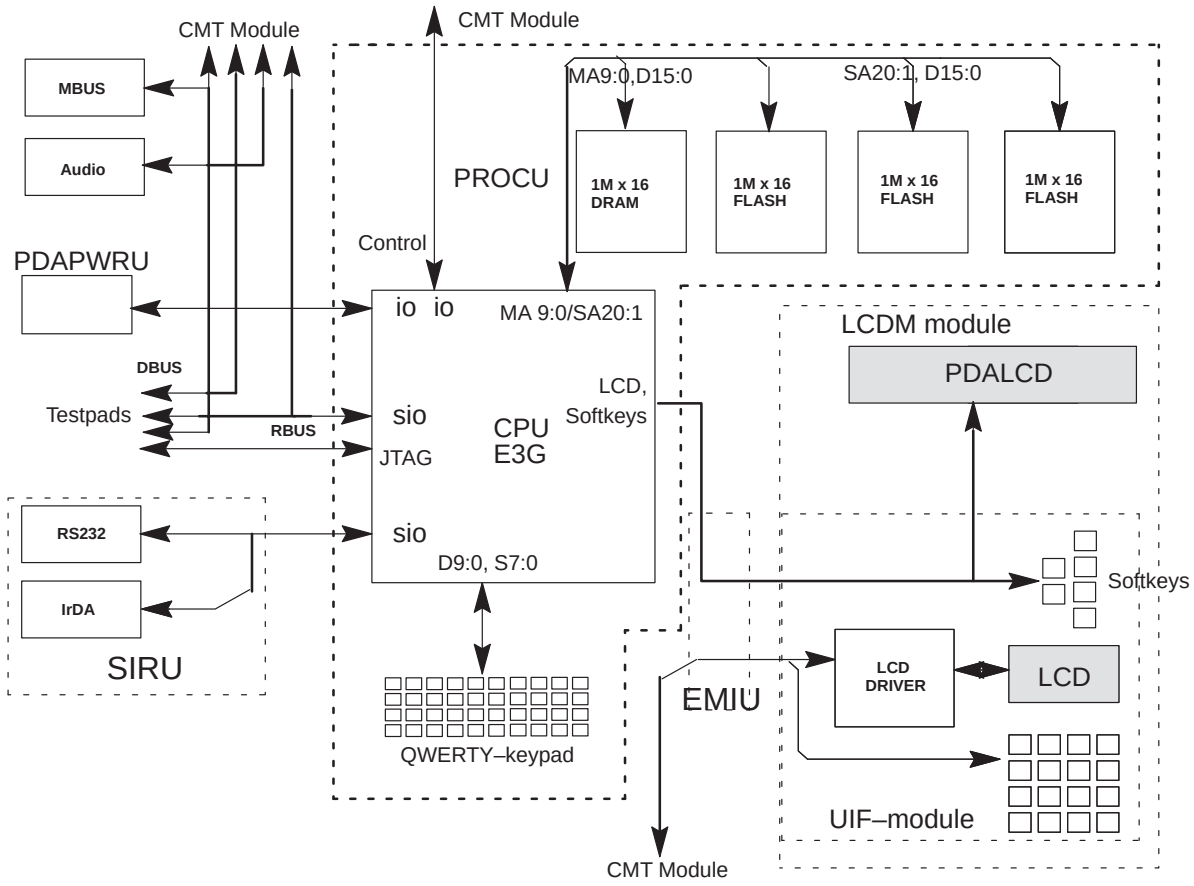

Figure 1. PDA Interconnection diagram

Modes of Operation

In principle there are four different operation modes

- fully on mode
- CPU core off mode (NAP)
- SUSPEND mode
- power supply off (Battery removed

The PDA module is always powered when a battery with adequate charge level is connected. Power saving in different modes is achieved by disabling clocks from functional blocks in an advanced manner. In the FULLY ON mode, all circuits are clocked, in the NAP mode, the CPU core is not clocked but all other circuits are clocked normally. In SUSPEND mode only the Real Time Clock (RTC) is clocked; DRAM is in self–refresh mode when the system is in SUSPEND mode. Asynchronous events, e.g., key presses and the lid being opened/closed, are able to wakeup the system from NAP and SUSPEND modes.

RTC is powered from the main battery as long as possible; in power supply OFF mode RTC is powered from the primary type of the backup battery.

DC Characteristics

Table 2. Supply Voltages and Power Consumption

Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
VB	5.75V	7.2V		CMT Software limit
	5.5V	7.2V	8.7 +/– 0.3V	CMT Hardware limit
	5.5V	7.2V	7.6 +/– 0.3V	CMT Hardware limit during a call
	4.9V	5.0V	5.1V	PDA Hardware limit
	5.9V	6.0V	6.1V	PDA Hardware limit cancel (remove VSYS shut-down)
VSYS	3.135V	3.3V	3.465V	regulator Imax=500mA
VCC5	4.825V	5.0V	5.175V	PDA FLASH pro-gramming voltage Imax=50mA
LCDVEE	17V	22V	25V	regulator Imax = 6mA PDALCD bias voltage
LCDVCC	3.135V	3.3V	3.465V	VSYS to LCD that can be switched off
VF (test)	11.4V	12V	12.6V	Flash programming voltage for CMT module
VL1	4.7V	4.85V	5.0V	CMT operating volt-age
VCHAR	10.0V	12V	13.0V	Charger specification without load (PDA –> CMT)
VCHARGER	10.0V 730mA	12V 780mA	13.0V 830mA	Charger specification (VCHAR in to 9000)

Table 3. DC characteristics of board to board connector Signals

Pin / Type.	Line Symbol	Mini-mum	Typi-cal / Nomi-nal (1)	Maxi-mum	Notes	
6 / UIF	BACKLIGHT	0V		0.7V	Output low, back-lights off	Display and key-pad illu-mination control
		4.7V	4.85V	5.0V	Output high, back-lights on	
8 / PDA, test	RBUSRxD	2.735 V			State ”1”	RBUS re-ceived data to CMT
				0.4V	State ”0”	
		3.6V	4.85V	5.0V	State ”1”	RBUS re-ceived data to CMT (Dur-ing CMT FLASH download
		0V	0.2V	0.7V	State ”0”	
9 / PDA, test	RBUSTxD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS trans-mitted data from CMT
		0V	0.2V	0.7V	State ”0”	
12 / UIF	XPWRON	0V	0V	0.7V	Input low, power on/ off	
			4.65V		Floating when inac-tive. A pull–up in PSL+.	
15 / SIM	BUZZEROUT	0V		0.7V	Output low, buzzer off	
		5.2V	7.2V	8.4V	Output high, buzzer on	
20–17 / UIF	COL(3:0)	0V		0.7V	Input low	keypad columns
		4.7V	4.85V	5.0V	Input high	
27–24 / UIF	UIF(3:0)	0V		0.7V	Output/Input low	keypad row lines/ display data lines
		4.7V	4.85V	5.0V	Output/Input high	
28 / UIF	UIF4	0V		0.7V	Output/Input low	keypad row read/write strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	

Pin / Type.	Line Symbol	Mini-mum	Typi-cal / Nomi-nal (1)	Maxi-mum	Notes	
29 / UIF	UIF5	0V		0.7V	Output/Input low	keypad row LCD driver register select
		4.7V	4.85V	5.0V	Output/Input high	
30 / UIF	UIF6	0V		0.7V	Output/Input low	enable strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	
32 / test	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
33 / test	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
34 / test	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS re-ceived data to 9000
		0V	0.2V	0.7V	State ”0”	
35 / test	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS trans-mitted data from 9000
		0V	0.2V	0.7V	State ”0”	
36 / sys-tem, test	MBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/ s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
38 / PDA	LIDOPEN	2.735 V			State ”1”	Lid status for CMT module
				0.2V	State ”0”	

(1) Nominal voltage will be 4.75–5 V

Table 4. DC characteristics of system connector signals

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
1,2	VCHARGER	10V	12V	13.0 V	Isink < 730mA	Charger voltage
		730mA	800mA	870mA	Uin < 10V	
3	SYSMBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35 V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
4	TESTMODEX	2.0V		3.635 V	State ”1”	Test SW activation
		–0.5V		0.8V	State ”0”	
8	SYSTxD	5.0V	7.3V		Output high level	External serial data from Responder
			–7.3V	–5.0 V	Output low level	
9	SYSRxD	–25V		1.2V	Input low level	External serial data to responder
		2.4V		25V	Input high level	

Table 5. DC characteristics of signals on test pads under the battery pack

Pad	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
E100	JTAGTDI	2.0V		3.635 V	State ”1”	JTAG data in
		–0.5V		0.8V	State ”0”	
E101	JTAGTCK	2.0V		3.635 V	State ”1”	JTAG clock
		–0.5V		0.8V	State ”0”	
E102	JTAGTMS	2.0V		3.635 V	State ”1”	JTAG mode control
		–0.5V		0.8V	State ”0”	

Pad	Line Symbol	Mini-mum	Typi-cal / Nomi-nal	Maxi-mum	Notes	
E103	JTAGTDO	2.735 V			State ”1”	JTAG data out
				0.4V	State ”0”	
E104	MBUS	0V		0.7V	Input low level	Isink<5mA-Baud rate 9600 bits/ s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35 V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
E106	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
E107	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
E108	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS re-ceived data to HP
		0V	0.2V	0.7V	State ”0”	
E109	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS trans-mitted data from HP
		0V	0.2V	0.7V	State ”0”	
8 / PDA, test	RBUSRxD	2.735 V			State ”1”	RBUS re-ceived data to CMT
				0.4V	State ”0”	
		3.6V	4.85V	5.0V	State ”1”	RBUS re-ceived data to CMT (Dur-ing CMT FLASH download
		0V	0.2V	0.7V	State ”0”	
E112	RBUSTxD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS trans-mitted data from CMT
		0V	0.2V	0.7V	State ”0”	
E113	TESTMODEX	2.0V		3.635 V	State ”1”	Test SW activation
		–0.5V		0.8V	State ”0”	

Table 6. DC characteristics of LCDM flex connector on PDA module

Pin / Type	Line Symbol	Mini-mum	Typi-cal / Nomi-nal	Maxi-mum	Notes	
6–3 / UIF	LCMUIF(3:0)	0V		0.7V	Output/Input low	keypad row lines/ display data lines
		4.65V		4.95V	Output/Input high	
7 / UIF	LCMUIF4	0V		0.7V	Output/Input low	keypad row read/write strobe for LCD driv-er
		4.65V		4.95V	Output/Input high	
8 / UIF	LCMUIF5	0V		0.7V	Output/Input low	keypad row LCD driv-er register select
		4.65V		4.95V	Output/Input high	
9 / UIF	LCMUIF6	0V		0.7V	Output/Input low	enable strobe for LCD driv-er
		4.65V		4.95V	Output/Input high	
14–11 / UIF	LCMCOL(3:0)	0V		0.7V	Output/Input low	Keypad column write
		4.65V		4.95V	Output/Input high	
15 / UIF	BACKLIGHTO	0V		0.7V	Output low, back-lights off	Display and key-pad illu-mination control
		4.65V	4.80V	4.95V	Output high, back-lights on	
16 / UIF	LCMXPRON	0V	0V	0.7V	Input low, power on/off	Power ON/OFF key
			4.65V		Floating when inac-tive. A pull–up in PSL+.	
21–18 / PDALCD	LCDD(3:0)			0.4 V	Output low	PDA LCD, Data lines
		2.735 V			Output high	
22 / PDALCD	LP			0.4 V	Output low	PDA LCD, Line pulse
		2.735 V			Output high	
23 / PDALCD	PCLK			0.4 V	Output low	PDA LCD, Pix-el clock
		2.735 V			Output high	

Table 6. DC characteristics of LCDM flex connector on PDA module (continued)

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Notes	
25 / PDALCD	FP			0.4 V	Output low	PDA LCD, Frame Pulse
		2.735 V			Output high	
26 / PDALCD	DISPON			0.4 V	Output low	PDA Display on control signal
		2.735 V			Output high	
31–29 / UIF	KEYD(2:0)			0.4 V	Output low	Keymatrix drive lines
		2.735 V			Output high	
33, 32 / UIF	KEYS(1:0)	– 0.5 V		0.8 V	Input low	Keymatrix sense lines
		2.0 V		3.635 V	Input high	

AC Characteristics

Table 7. Audio Signals

Pin / Type (1, 2)	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	
42 / B2B	EXTEAR		130 mV_{rms}	500 mV_{rms}	
41 / SC	SYSEXTMIC		200 mV_{rms}	530 mV_{rms}	
42 / SC	SYSEXTEAR		130 mV_{rms}	500 mV_{rms}	

Note 1. B2B = Board to board connector between PDA and CMT modules
Note 2. SC = System Connector

Connectors

Connectors Inside Transceiver Unit

Table 8. PDA board to board connector

Signal Name	Pin	Notes
VB	1, 44	Battery voltage
GND	2, 5, 7, 10, 13, 21, 22, 23, 37, 39, 40	Ground
PHFMICN	3	PHF microphone (negative node)
PHFMICP	4	PHF microphone (positive node)
BACKLIGHT	6	Backlights on/off
RBUSRxD	8	RBUS receive (CMT <– PDA or test)
RBUSTxD	9	RBUS transmit (CMT –> PDA or test)
VL1	11	Logic supply voltage (4.75–5V)
XPWRON	12	Power key (active low)
VCHAR	14,31	Battery charging voltage. 2 pins needed
BUZZEROUT	15	Buzzer signal to buzzer on SIM module
VF	16	Programming voltage for flash.
COL(3:0)	20–17	Lines for keypad write
UIF(3:0)	27–24	Lines for keypad read and LCD–controller data
UIF4	28	Line for keypad read and LCD–controller read/ write strobe
UIF5	29	Line for keypad read and LCD–controller data/ instruction register selection
UIF6	30	LCD–controller enable strobe
DCLK	32	DBUS–data clock
DSYNC	33	DBUS–data bit sync clock
RDA	34	DBUS received data from the accessories
TDA	35	DBUS transmit data to the accessories
MBUS	36	Serial bidirectional data and control between the handphone and accessories.
LIDOPEN	38	Lid status for CMT module

Table 8. PDA board to board connector (continued)

Signal Name	Pin	Notes
EXTMIC	41	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
EXTEAR	42	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
AGND	43	Analog ground for accessories. Connected directly to digital ground on the PCB.

Table 9. HFMIC Connector

Signal Name	Pin	Notes
PHFMICN	1	Negative MIC input
PHFMICP	2	Positive MIC input

Table 10. LCDM module flex connector on PROCU

Signal Name	Pin	Notes
GND	10, 17, 24	Ground or VB (flex material dependent)
VB	1	Power lines for backlight LEDs
VL1	2	Phone LCD power
LCMUIF(3:0)	6, 5, 4, 3	Lines for keypad read and LCD–controller data
LCMUIF4	7	Line for keypad read and LCD–controller read/write strobe
LCMUIF5	8	Line for keypad read and LCD–controller data/instruction register selection
LCMUIF6	9	LCD–controller enable strobe
LCMCOL(3:0)	14, 13, 12, 11	Lines for keypad write
BACKLIGHTO	15	Backlights on/off (controll)
LCMXPRON	16	Power ON/OFF key
LCDD(3:0)	21, 20, 19, 18	PDA LCD Data lines
LP	22	PDA LCD, Line pulse
PCLK	23	PDA LCD, Pixel clock
FP	25	PDA LCD, Frame Pulse
DISPON	26	PDA Display on control signal
LCDVCC	27	PDA LCD Logic voltage
LCDVEE	28	PDA LCD Bias voltage (+21V)
KEYD(2:0)	31, 30, 29	Keymatrix drive lines
KEYS(1:0)	33, 32	Keymatrix sense lines

Connectors Out of Transceiver Unit

Table 11. System Connector

Signal Name	Pin	Notes
VCHARGER	1, 2	Battery charging voltage.
SYSMBUS	3	Serial bidirectional data and control between the handphone and accessories.
TESTMODEX	4	Test SW activation
SYSEXTMIC	6	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
SYSEXTEAR	7	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
SYSTXD	8	External serial data from the 9000
SYSRXD	9	External serial data to 9000
AGND	10	Analog ground for accessories. Connected directly to digital ground on the PCB.
GND	5, 11, 12	Charger and digital ground.

Table 12. Test pads under the battery pack

Signal Name	Pad	Notes
JTAGTDI	E100	JTAG data in
JTAGTCK	E101	JTAG clock
JTAGTMS	E102	JTAG mode control
JTAGTDO	E103	JTAG data out
MBUS	E104	Serial bidirectional data and control between the handphone and accessories.
VF	E105	Flash programming voltage
DCLK	E106	DBUS–data clock
DSYNC	E107	DBUS–data bit sync clock
RDA	E108	DBUS received data from the accessories
TDA	E109	DBUS transmit data to the accessories
GND	E110	Signal ground
RBUSRxD	E111	RBUS receive (CMT <– PDA or test)
RBUSTxD	E112	RBUS transmit (CMT –> PDA or test)
TESTMODEX	E113	PDA test SW activation

Internal Signals and Connections

Table 13. Signals Between PROCU and power supply unit

Signal Name	Function	Notes
LCDPWM	PWM signal for LCD voltage control	LCD contrast control
LCDVCCON	LCD Vcc on/off	
LCDVEEON	LCD Vee on/off	
PWRGOOD	Reset signal for CPU	VSYS valid
VBACK	Backup battery voltage to RTC	
5VPDX	5V regulator powerdown	

Functional Description

Introduction

Intel E3G is 386 based core with all needed peripherals on same chip. E3G is used to execute all applications, GEOS, DOS, BIOS, and TFFS.

Clocking Scheme

Actual clock signals are not routed to any other chip than previously mentioned E3G. All clocks are generated from a 32.768 kHz chrystal with PLL's integrated to the E3G CPU chip.
System clock rates are as follows:

CPU core	23.96 MHz
UART's	1.84MHz
8254 Timer	1.198MHz
RTC	32.768kHz

Reset and Power Management

Power good (PWRGOOD) signal from PDAPWRU module is used as a system reset. Both PDA and CMT modules power management system is implemented with special hardware in close co–operation with operating system.

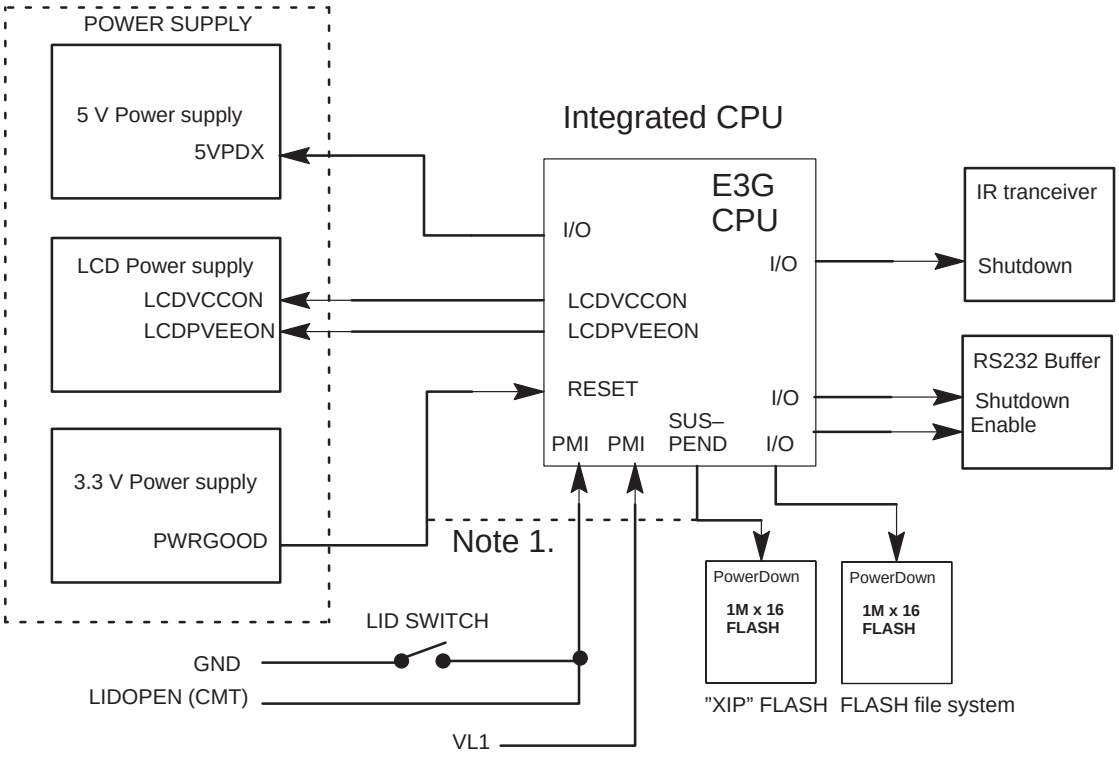

Figure 2. Reset and power management block diagram

PDA power management principle.

Operating voltage is always ON on the PDA module when battery is connected and charge level on the battery is above PDA power supply limit (HW cutt–off). When battery is connected voltage must rise over 'PDA HW limit cancel voltage' to start CPU power–up. Power consumption reduction is achieved by stopping clocks from the system (stable state power consumption in CMOS logic is really small).
From CMT point of view PDA module have only two states PDA_ON and PDA_SUSPEND illustrated in figure 3. When PDA is in PDA_SUSPEND state it takes about 500 ms (max) Note 1. to wake it up. During the wakeup period all messages from CMT are discarded. When PDA is in PDA_ON it wakes up immediately (max few microseconds) and messages are not discarded. CMT is never able to be ON when PDA is not able to wakeup because CMT is switched OFF before PDA when battery level is falling. See Figure 5 that depicts battery charge levels and its effects to PDA and CMT modules.

Note 1. On A–3 CPU version startup time in low temperatures is up to 20s

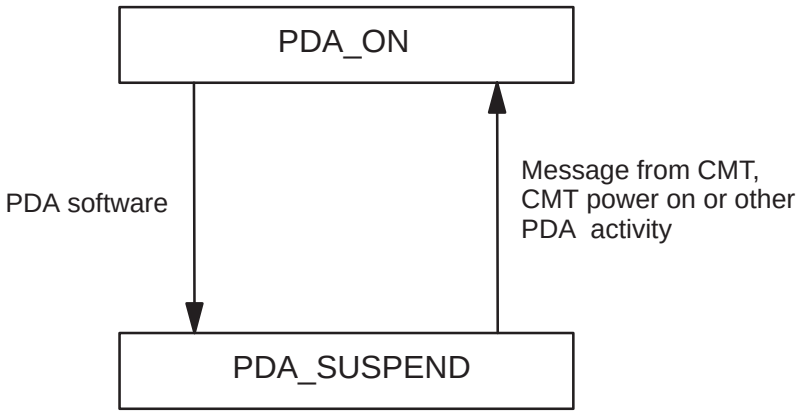

Figure 3. PDA power states from CMT point of view.

The PDA knows whether CMT is on or off by monitoring VL1. It gets information about battery level by asking for battery level from the CMT.

The PDA is able to switch CMT to the CMT_PDA_REQUEST_SERVICE state.

CMT power management principle.

The goal is that existing power management scheme of CMT in HD841 is changed as little as possible. CMT module has power switch that works as on normal DCT1 cellular phones. The CMT_PDA_REQUEST_SERVICE state is implemented to support requests from PDA even when CMT is switched off. RF is not activated when CMT is on the CMT_PDA_REQUEST_SERVICE state. If CMT_PDA_REQUEST_SERVICE state is activated by PDA, CMT switches itself off after requested action is done. CMT power states are illustrated in Figure 4.

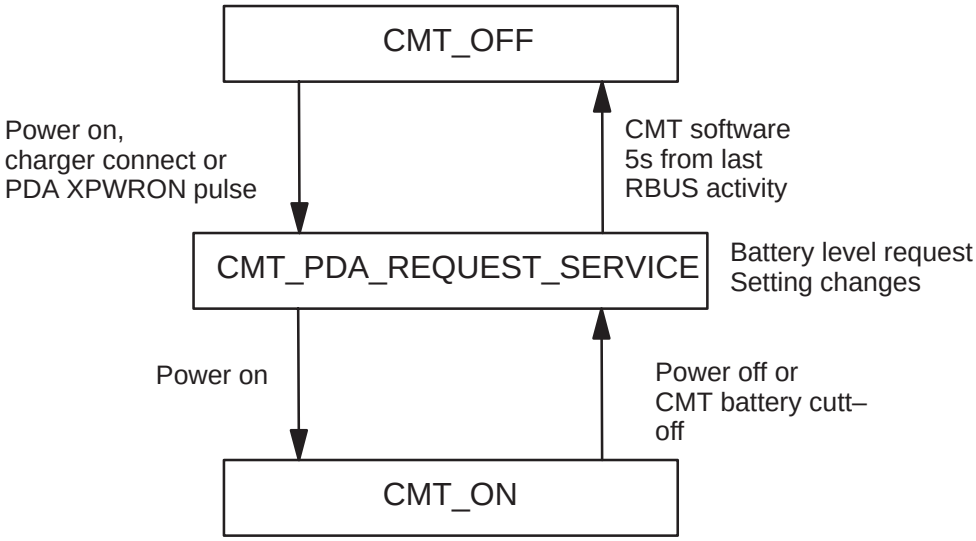

Figure 4. CMT power states from PDA point of view.

Battery charge level limits on CMT and PDA

Figure 5 (overleaf) shows an example of combined CMT and PDA critical battery levels, measurement accuracy (+/– 50mV). There are two kind of limits most of which are implemented in software.

The AD converter, located in the CMT module, is used as a source for battery level values needed by both CMT and PDA software. PDA gets battery level information from the AD converter via ECI messages. The CMT HW limit, PDA HW cut–off and Battery protect circuit cut–off are implemented in hardware and actions are taken without notice to any software.

The following limits are based on battery level values read from the AD converter; decisions are made by software.

- *Battery low level warning 1*
  If CMT is ON this warning is generated by CMT sending a message to PDA when warning 1 is triggered. If CMT is OFF, PDA must generate this warning itself.
- *CMT battery cut–off*
  CMT switches itself off when battery level has fallen below this level.
- *Battery low level warning 2*
  PDA generates this warning when the battery level value read from CMT has fallen below this level.
- *PDA limit (Data save)*
  PDA saves all user data and disables PDA when the battery level is below this level.

The following limits are implemented in hardware:

- *CMT HW limit*
  CMT power supply switches itself off.
- *PDA HW cut–off*
  PDA power supply switches itself off.
- *Battery protect circuit cut–off*
  A circuit in the battery package switches power off from battery output pads.

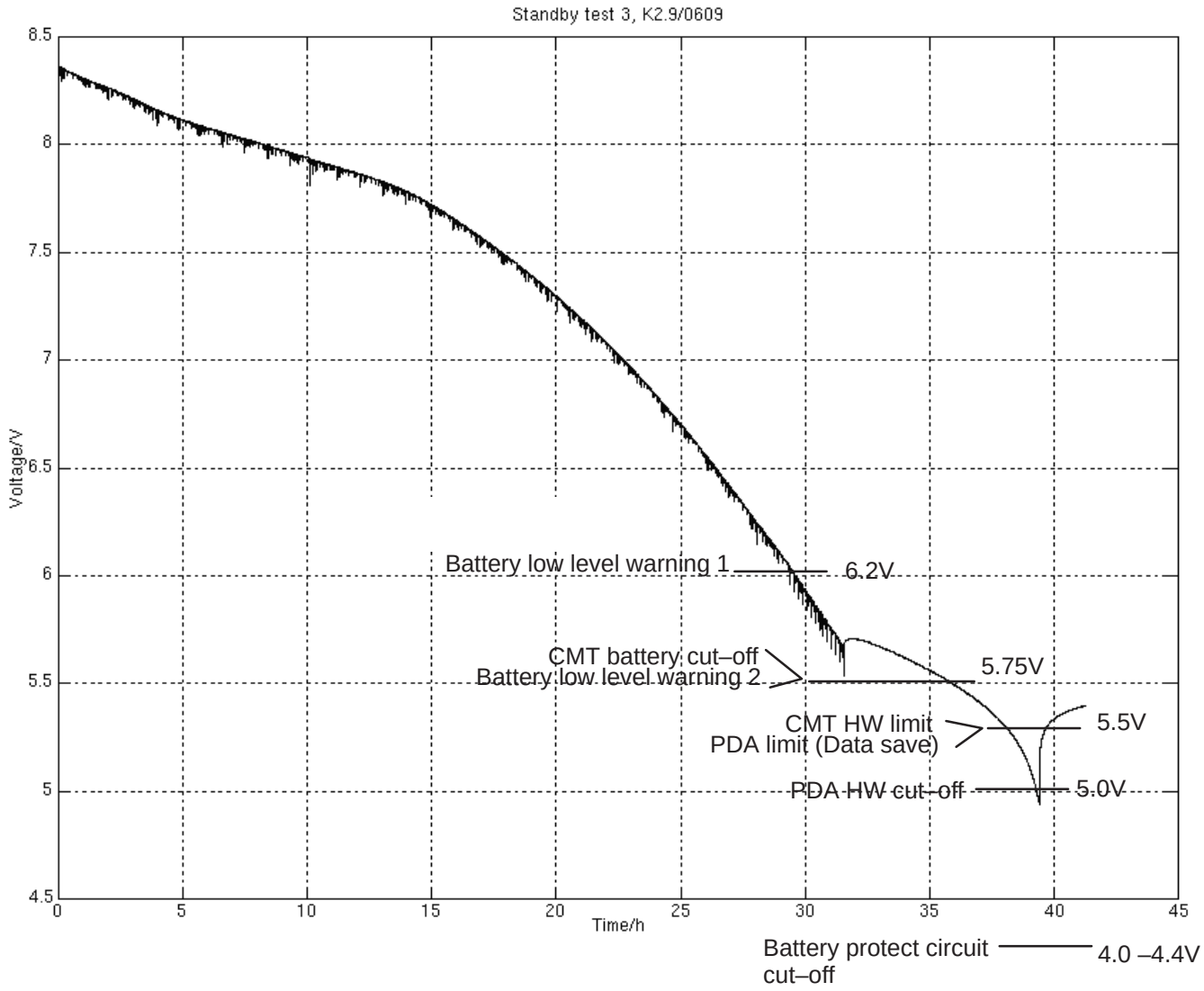

Figure 5. Discharge voltage curve of battery (two Li–Ion cells) in stadby

EMIU

This module contains only passive components to suppress EMI generated voltages on external signal lines.

Note 1. B2B = Board to board connector between PDA and CMT modules

Table 14. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
BACKLIGHTI	Backlights on/off (control)	B2B / Back-light
KEYDI(2:0)	Keymatrix drive lines	PROCU / KEYD(2:0)
KEYSI(1:0)	Keymatrix sense lines	PROCU / KEYS(1:0)
LCDD(3:0)	PDA LCD Data	PROCU / LCDD(3:0)
DISPONI	PDA LCD Display on control signal	PROCU / DISPON
FPI	PDA LCD Frame Pulse	PROCU / FP
PCLKI	PDA LCD Pixel Clock	PROCU / PCLK
LPI	PDA LCD Line Pulse	PROCU / LP
PHFMICNI	Negative Hands Free MIC input	B2B / PHFMICN
PHFMICPI	Positive Hands Free MIC input	B2B / PHFMICP
COL(3:0)I	Lines for keypad write	B2B / COL(3:0)
UIF(3:0)I	Lines for keypad read and LCD–controller data	B2B / UIF(3:0)
UIF4I	Line for keypad read and LCD–controller read/write strobe	B2B / UIF4
UIF5I	Line for keypad read and LCD–controller data/insruction register selection	B2B / UIF5
UIF6I	LCD–controller enable srobe	B2B / UIF6
MBUSI	Serial bidirectional data and control between the handphone and accesseries	B2B / MBUS
EXTMICI	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT	B2B / EX-TMIC
EXTEARI	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.	B2B / EX-TEAR

Note 1. LCMCON = LCD module connector on PDA module

Note 2. MICCON = Hands–free microfone connector on PDA module
Note 3. SC = System Connector

Table 15. External Signals and Connections, Outputs

Signal Name	Signal description	To (1,2,3)
BACKLIGHTO	Backlights on/off (control)	LCDMCON / BACKLIGH-TO
KEYDO(2:0)	Keymatrix drive lines	LCMCON / KEYD(2:0)
KEYSO(1:0)	Keymatrix sense lines	LCMCON / KEYS(1:0)
LCDDO(3:0)	PDA LCD Data	LCMCON / LCDD(3:0)
DISPONO	PDA LCD Display on control signal	LCMCON / DISPON
FPO	PDA LCD Frame Pulse	LCMCON / FP
PCLKO	PDA LCD Pixel Clock	LCMCON / PCLK
LPO	PDA LCD Line Pulse	LCMCON / LP
PHFMICNO	Negative Hands Free MIC input	MICCON / 1
PHFMICPO	Positive Hands Free MIC input	MICCON / 2
COL(3:0)O	Lines for keypad write	LCDMCON / LCDMCOL(3:0)
UIF(3:0)O	Lines for keypad read and LCD–controller data	LCDMCON / LCDMUIF(3: 0)
UIF4O	Line for keypad read and LCD–controller read/write strobe	LCDMCON / LCDMUIF4
UIF5O	Line for keypad read and LCD–controller data/insruction register selection	LCDMCON / LCDMUIF5
UIF6O	LCD–controller enable srobe	LCDMCON / LCDMUIF6
MBUSO	Serial bidirectional data and control between the handphone and accesseries	SC / SYSM-BUS
EXTMICO	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in HP	SC / SY-SEXTMIC
EXTEARO	External audio output to accessories or handsfree speaker. 100kΩ pull–down in HP to turn on the junction box.	SC / SY-SEXTEAR

PROCU

The Processing unit contains integrated Intel E3G CPU (CPU and peripherals on the same chip), two types of memory circuits (DRAM, FLASH), a 22–bit address bus (26 bit internally), and a 16–bit data bus.

PROCU functions:

– GEOS, DOS, BIOS, TFFS and GEOS application platform
– user interface functions
– external interfaces (IrDA and RS232)
– power management
– self–test, production testing, and maintenance

Technical specifications

Table 16. External Signals and Connections, Inputs

Signal Name	Signal description	From
VSYS	System voltage 3.3V	PDAPWRU
VCC5	5V for FLASH and RBUS	PDAPWRU
VB	Battery voltage	B2B / VB
VL1	CMT operating voltage	B2B / VL1
PWRGOOD	Reset signal for CPU	PDAPWRU
VBACK	Backup battery voltage to RTC	PDAPWRU
RBUSTXD	RBUS transmit of CMT	B2B / RBUSTXD
RSRXD	Serial data to PDA module	SIRU
TESTMODEX	PDA test SW activation	Test pad / E113
JTAGTDI	JTAG data in	Test pad / E100
JTAGTCK	JTAG clock	Test pad / E101
JTAGTMS	JTAG mode control	Test pad / E102
KEYS(1:0)	Keymatrix sense lines	EMIU

Table 17. External Signals and Connections, Outputs

Signal Name	Signal description	To
LIDOPEN	Lid status for CMT module	B2B / LIDO-PEN
LCDVCCON	LCD Vcc on/off	PDAPWRU
LCDVEEON	LCD Vee on/off	PDAPWRU
LCDPWM	PWM signal for LCD voltage control	PDAPWRU

Table 17. External Signals and Connections, Outputs (continued)

Signal Name	Signal description	To
5VPDX	5V regulator powerdown	PDAPWRU
XPWRON	Power key (active low)	B2B / XPOWER-ON, LCMCON / LCMXPOW-ERON
RBUSRXD	RBUS receive of CMT (CMT <– PDA)	B2B / RBUSRXD
RSTXD	Serial data from PROCU module	SIRU
RSENX	RS buffer enable	SIRU
RSSHDX	RS buffer shutdown	SIRU
IRSHD	IR tranceiver shutdown	SIRU
JTAGTDO	JTAG data out	Test pad E103
BUZZEROUT	Buzzer signal to buzzer on SIM module	B2B / BUZZER-OUT
LP	PDA LCD Line Pulse	EMIU
PCLK	PDA LCD Pixel Clock	EMIU
FP	PDA LCD Frame Pulse	EMIU
LCDD(3:0)	PDA LCD Data	EMIU
DISPON	PDA display on control signal	EMIU
KEYD(2:0)	Keymatrix drive lines	EMIU

Block description

– PROCU Memories

Two types of memory is used: DRAM, and FLASH (ROM). The E3G CPU has a 22 bits (26 bit internal) wide external address bus A(21:0) and an 16–bit data bus. The address bits A(25:11) are used for chip select decoding. The decoding is done internally on the E3G CPU.

PROCU memory map is illustrated in figures 1 and 2 and in Table 31

DRAM (70 ns) is refreshed only when main battery is connected. As long as the main battery has power and is connected all the DRAM data stays valid. When the main battery is removed all the DRAM data is lost.

All application data is saved to nonvolatile FLASH memory under control of flash file system (TFFS by M–Systems). Application status is not stored.

DRAM area is composed of a single 1M x 16 bit chip. The access time of 70 ns enables zero wait–state page access and one wait–state page fault.

FLASH memory is used for two purposes on this device. Two 1M x 16 bit chips (75 ns) are used for BIOS, DOS, GEOS and applications this memory is usually called XIP FLASH. A 1M x 16 bit chip (120 ns) is used to save user data. This memory device is handled by FLASH file system. From application point of view this memory is accessed like hard disk using INT13 functions. 75 ns FLASH device needs one wait–state and 120 ns device two wait–states.

FLASH devices are equipped with Reset/Power down pin (RP#) which can be used to place devices in a Deep PowerDown state. RP# pin of two XIP FLASH devices is connected to SUSPEND pin of E3G. SUSPEND# pin is active when E3G is in SUSPEND mode and internal PLL's are not runnig. RP# pin of the FLASH device under TFFS is connected to a GPIO pin and it is controlled by TFFS. TFFS and RS232 flash download softwares are able to control 5V power supply powerdown. There is 100us delay needed between 5V power up and write command.

1 Mbyte of address space is directly addressable by the CPU (conventional memory). Any additional memory is accessed via Expanded Memory System EMS . EMS system follows LIM 4.0 specification.

Memory Map

Table 18. Memory Map

000000 00FFFF	Interrupt Vector, DOS data (DRAM)
010000 07FFFF	GEOS heap (DRAM)
09E400 0A03FF	True FFS data (DRAM)
0A0400 0A05FF	BIOS data (DRAM)
0A0600 0AFFFF	Video buffer (DRAM)
0B0000 0B3FFF	EMS page 0 (True FFS & GEOS ROM disk)
0B4000 0B7FFF	EMS page 1 (XIP page 2) EMS register

Table 18. (continued) Memory Map

0B8000 0B2BFFF	EMS page 2 (XIP page 1) EMS register
0BC000 0BFFFF	EMS page 3 (Fixed GEOS XIP) EMS register
0C0000 0ECBFF	GEOS XIP (XIP FLASH 1.) Double mapped area
0ECC00 0F77FF	ROM–DOS (XIP FLASH 1.) Double mapped area
0F7000 0FBFFF	True FFS (XIP FLASH 1.) Double mapped area
0FC000 0FFFFF	BIOS (XIP FLASH 1.) Double mapped area
100000 1FFFFF	SWAP/RAMDISK (Uppermost meg of DRAM)
200000 24FFFF	SWAP/RAMDISK (DRAM Roll–Over. The DRAM area that is ”under” double mapped XIP FLASH and EMS registers.)
3A00000 3BFFFFF	True FFS FLASH area
3C00000 3DFFFFF	GEOS and applications (XIP FLASH 2)
3E00000 3EBFFFF	GEOS and applications (XIP FLASH 1)
3EC0000 3EECBFF	GEOS XIP (XIP FLASH 1)
3EECC00 3EF77FF	ROM–DOS (XIP FLASH 1)
3EF7800 3EFC7FF	True FFS (XIP FLASH 1)
3EFC800 3EFFFFF	BIOS (XIP FLASH 1)

Table 18. (continued) Memory Map

3F00000 3FFFBFF	DOS ROM–DISK about 80k GEOS and applications (XIP FLASH 1) Upper non–resident XIP
3FFFC00 3FFFF9F	Reserved for manufacturing and aftersales data
3FFFFA0 3FFFFAF	PDA_PROD_HW_VERSION
3FFFFB0 3FFFFBF	PDA_PROD_HW_CODE
3FFFFC0 3FFFFCF	PDA_PROD_HW_NUMBER
3FFFFD0 3FFFFEF	PDA_SW VERSION
3FFFFF0 3FFFFFB	Jump to BIOS code jump command
3FFFFFC 3FFFFFF	Image checksum

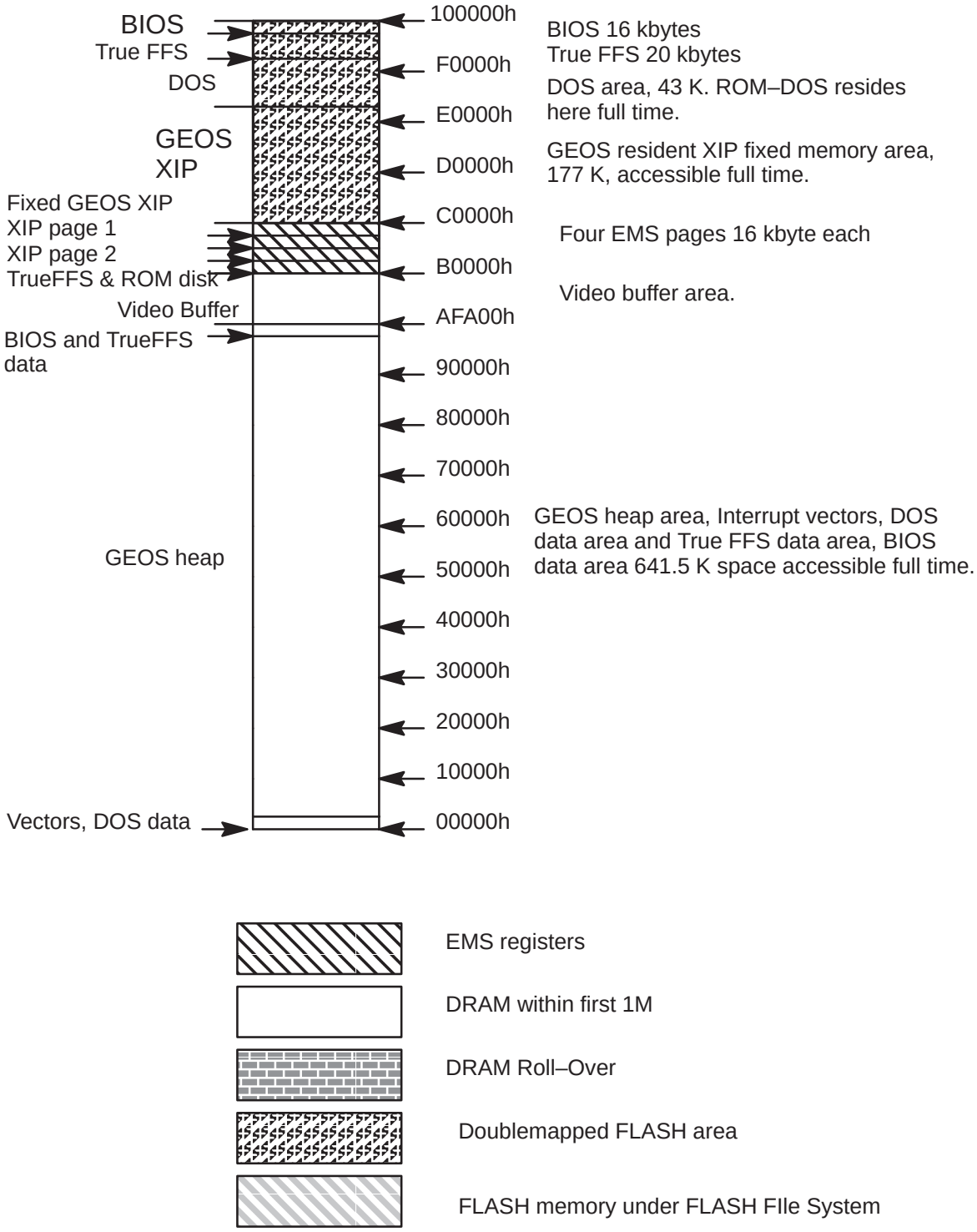

Figure 6. PROCU memory map part 1

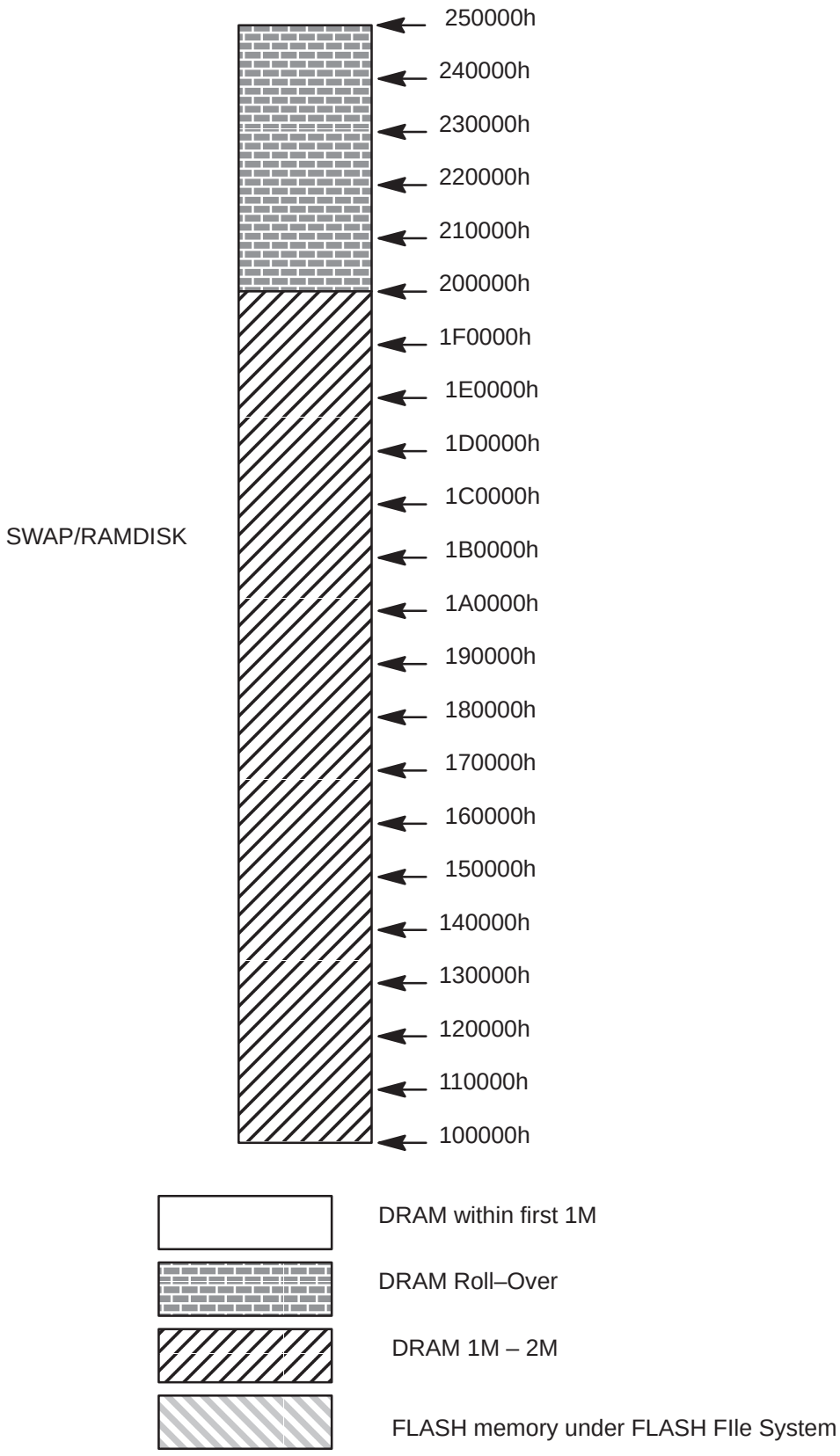

Figure 7. PROCU memory map part 2

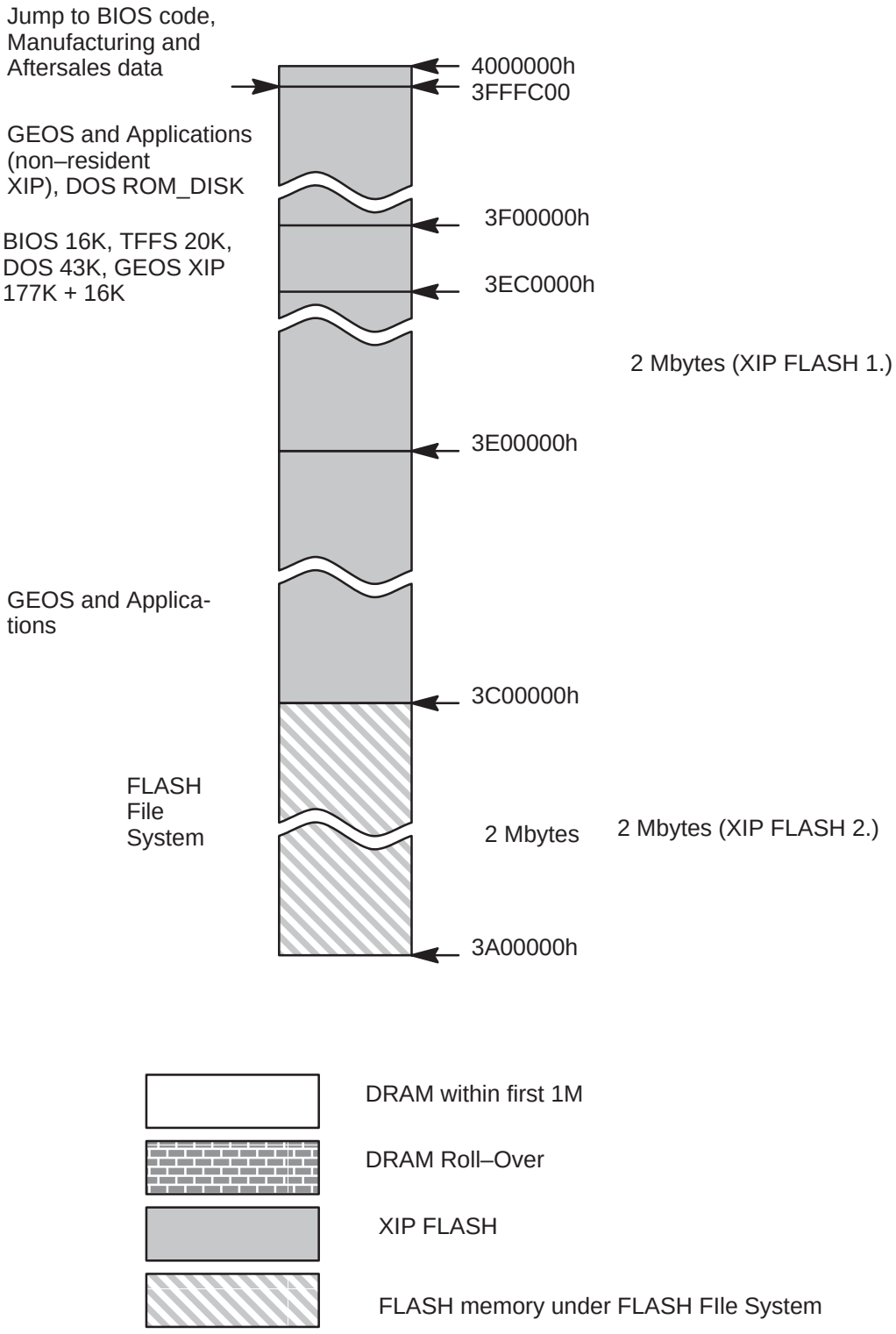

Figure 8. PROCU memory map part 3

– Chip selects

E3G CPU has four programmable chip selects. Size of the memory block can be defined with 2K resolution. Start address can be changed in 2K boundaries. These chip selects have independent programmable wait states (0–64).

Table 19. FLASH Chip Select Generation

A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	CHIP SELECT	NOTES
1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	UCS XIP FLASH 1.	
0	0	0	0	0	0	1	1	X	X	X	X	X	X	X	UCS XIP FLASH 1.	Double map-ping
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	CS0 XIP FLASH 2.	
1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	CS1 RFD FLASH 1.	

DRAM controller enables shadowing in the area of 640KB – 1MB in 16–Kbyte granularity. Each block of memory can be configured as being disabled, read–only, write–only, or read/write. Unused memory in the area of 640KB – 1MB can be rolled over in 64–Kbyte granularity. Roll–over base is selectable in 512–Kbyte granularity.

– FLASH programming

PDA module FLASH memories can be programmed in two ways. During the manufacturing JTAG interface of the E3G CPU is used to download FLASH image to FLASH devices. For aftersales and R&D purposes BIOS is equipped with FLASH download capability via RS232. JTAG method is needed at aftersales as a backup.

During the manufacturing it is not possible to use any download method that needs CPU involvement because there is no any program code for execution on the device. JTAG interface was selected for this purpose because it exists on the E3G CPU and it is a standard. In principle JTAG interface is able to set CPU signals (address, data, etc.) to requested state. By changing signal values in reasonable manner FLASH writing is possible. Special hardware is needed for JTAG FLASH download during manufacturing as well as for aftersales purposes. JTAG FLASH download system is integrated to PTS and maintenance software.

RS232 FLASH load can be done with standard PC with a serial port and FLASH loading software. Upload is also possible with this software. On the PDA module RS232 FLASH download software is part of the BIOS. RS232 FLASH download commands are integrated to maintenance software.

FLASH programming voltage is generated on PDAPWRU. FLASH memory content validity can be checked by calculating error check code and comparing it to precalculated one.

– PROCU – PDAPWRU

PDAPWRU generates 3.3V VSYS for overall system usage and 5V for FLASH programming. FLASH programming voltage can be switched off with 5VPDX signal when it is not needed. Switchmode powersupplies are used for VSYS and LCD Vee. LCD display contrast control (bias) is generated by PWM unit in E3G CPU. This signal controls LCD Vee power supply on PDAPWRU. LCD bias and LCD logic voltages can be switched on and off by PROCU with LCDVEE and LCDVCC signals. PDAPWRU generates power good (PWRGOOD) signal for PROCU reset purpose. VBACK is always available for real time clock.

– PROCU – LCDM

640 x 200 LCD screen (8 actual grey scales) on LCDM is controlled by PROCU. Soft keys and scroll keys on LCDM module are connected to the keyboard controller on PROCU.

– PROCU – SIRU

IrDA transceiver and RS232 buffer are located to SIRU. Same RXD and TXD lines are used for both devices. When the device is not used the transmit line must be in high impedance state. Only one device is allowed to be enabled at a time. RS buffer have two control signals. RSENX to enable transmit line and RSSHDX to enable charge pump. IrDA tranceiver is enabled with IRSHD signal. External RS232 signals meet EIA/TIA–232 specification.

– PROCU – EMIU

EMI Unit is passive unit to reduce EMI noise on the lines that are located out of the shielding.

I/O usage on E3G CPU

The E3G CPU have configurable I/O pins that are used like described on Table 21.

Table 20. I/O usage on E3G CPU

Signal name	E3G CPU pin	Polarity	Reset value
PWRGOOD	RESET#	H = Power good	– (In)
5VPDX	PMI2 / P45	L = Shut down	L
TESTMODEX (Input)	DTR0# / P02	L = Test mode	– (In)
IRSHD	RI1# / P13	H = Shut down	H
RSSHDX	DSR0# / P00	L = Shut down	H
RSENX	CTS0# / P04	L = Enabled	H
XPWRON	PMI3 / P44	H (pulse) => CMT ON	L
FLASHPD1X	SUSPEND#	L = Shut down	H
FLASHPD2X	RI0# / P03	L = Shut down	H
FLASHWP1X	DCD0# / P01	L = Protected	H
FLASHWP2X	CTS1# / P15	L = Protected	H
LCDVCCON	LCDVCCON	H = Vcc ON	L
LCDVEEON	LCDVEEON	H= Vee ON	L
DISPON	DISPON	H = Display ON	L
”LID”	PMI0	H = Lid open	– (In)
VL1	PMI1	H = CMT ON	– (In)

I/O map

All chipselects are generated in the E3G.

Table 21. I/O Map

Device	Address	Note
PIC0	0020 – 0021	Standard PC compatible
PIC0	F022h	Edge / Level control E3G Specific
Timers 0 – 2	0040h – 0043h	Standard PC compatible
Port B	0061h	Standard PC compatible
RTC Offset	0070h	Standard PC compatible
RTC Data	0071h	Standard PC compatible
Port 92	0092h	Standard PC compatible
PIC1	00A0h – 00A1h	Standard PC compatible
PIC1	F0A2h	Edge / Level control E3G Specific
COM2	02F8h – 02FF	Standard PC compatible
COM1	03F8h – 03FF	Standard PC compatible
DRAM controller	F300h – F323h	E3G Specific
IRDA Select Register	F3F8h – F3F9h	E3G Specific

Table 21. I/O Map (continued)

Device	Address	Note
Chip Select Unit	F400h – F463h	E3G Specific
E3G Clock Unit	F800h, F87Bh	E3G Specific
E3G Bus Control Unit	F810h – F813h	E3G Specific
E3G Chip Configuration Registers	F820h – F825h	E3G Specific
E3G I/O Ports Unit	F860h – F87Bh	E3G Specific
E3G LCD Controller	F900h – F925h	E3G Specific
E3G PWM Unit	FC00h – FC01h	E3G Specific
E3G EMS Registers	FC10h – FC1Bh	E3G Specific
E3G Key Scan Unit	FC30h – FC39h	E3G Specific
E3G Power Management	FCA0h – FCB3h	E3G Specific

Interrupt map

The interrupt control unit inside the E3G contains two 8259A modules, connected in a cascade mode.

Table 22. Interrupt map

PC INT#	IRQx	Vector (hex)	Name	PC use
2	NMI	8	PMU INT	Parity Error / IO Check
8	IRQ0	20	Timer 0	same
9	IRQ1	24	Key Scan logic	8042 Keyboard
A	IRQ2	28	cascade vector	same
B	IRQ3	2C	COM2 (RBUS)	same
C	IRQ4	30	COM1 (RS232)	same
70	IRQ8	1C0	RTC	same
72	IRQ10	1C8	Timer 1 (Not used but available)	ISA

Main components

– E3G CPU

80386 based CPU. Static design. Using external clock source maximum clock rate 33MHz. With internal PLL's 23.96MHz. All needed peripherals are integrated to the same chip. Peripherals are as follows:

- Two cascaded Interrupt Controllers (8259A), DOS compatible
- Three programmable Timer/Counters, 8254 standard
- DRAM bus controller, no external buffers or multiplexers needed
- Chip select unit
- Real time clock (RTC)
- Two 16550 UART's with 16–byte FIFO's
- IrDA signal conditioning and RS232/IrDA select
- LCD controller (640 x200 8 actual grey scales)
- Pulse Width Modulator Unit
- 8 x 10 keyboard scan unit
- System power management unit
- Expanded Memory Specification (EMS) Unit
- 32 KHz Oscillator with Phase Locked Loop circuits to generate all needed frequencies
- JTAG (IEEE 1149.1) Boundary scan testing capability

E3G CPU is described in details in E3G EXTERNAL ARCHITECTURE SPECIFICATION, Intel Corporation 5000 West Chandler Blvd. Chandler, AZ 85226

– 1M*16bit FLASH memory 75 ns

- Intel 28F016SV 065
- 75 ns maximum read access time
- SMART voltage device with 5 Volt programming
- Used to store all program code
- 1 Million Erase Cycles Per Block
- Deep power down mode

- 1M*16bit FLASH memory 120 ns
    - Intel 28F016SV 070
    - 120 ns maximum read access time
    - SMART voltage device with 5 Volt programming
    - Used to store application data under FLASH File System
    - 1 Million Erase Cycles Per Block
    - Deep power down mode

- 1M*16bit DRAM memory
    - 70 ns maximum access time
    - Fast Page Mode
    - CAS before RAS refresh
    - CAS before RAS self refresh
    - Refresh block size 1K

- QWERTY–keypad
    - Hard top rubber keymat with carbon contacts
    - 56 QWERTY keys and 9 function keys
    - Key ON resistance < 1kohm
    - VT100 emulation compatibility keys included

PDAPWRU

Technical Description

The power block creates supply voltages for the PROCU and LCDM, generates reset signal for CPU and contains LCD contrast control and enable circuits. Input filter is required to reduce input noise of switching regulators. Back–up battery keeps RTC alive when main battery is not connected. System voltage is present allways until battery voltage drops below 5.0V.

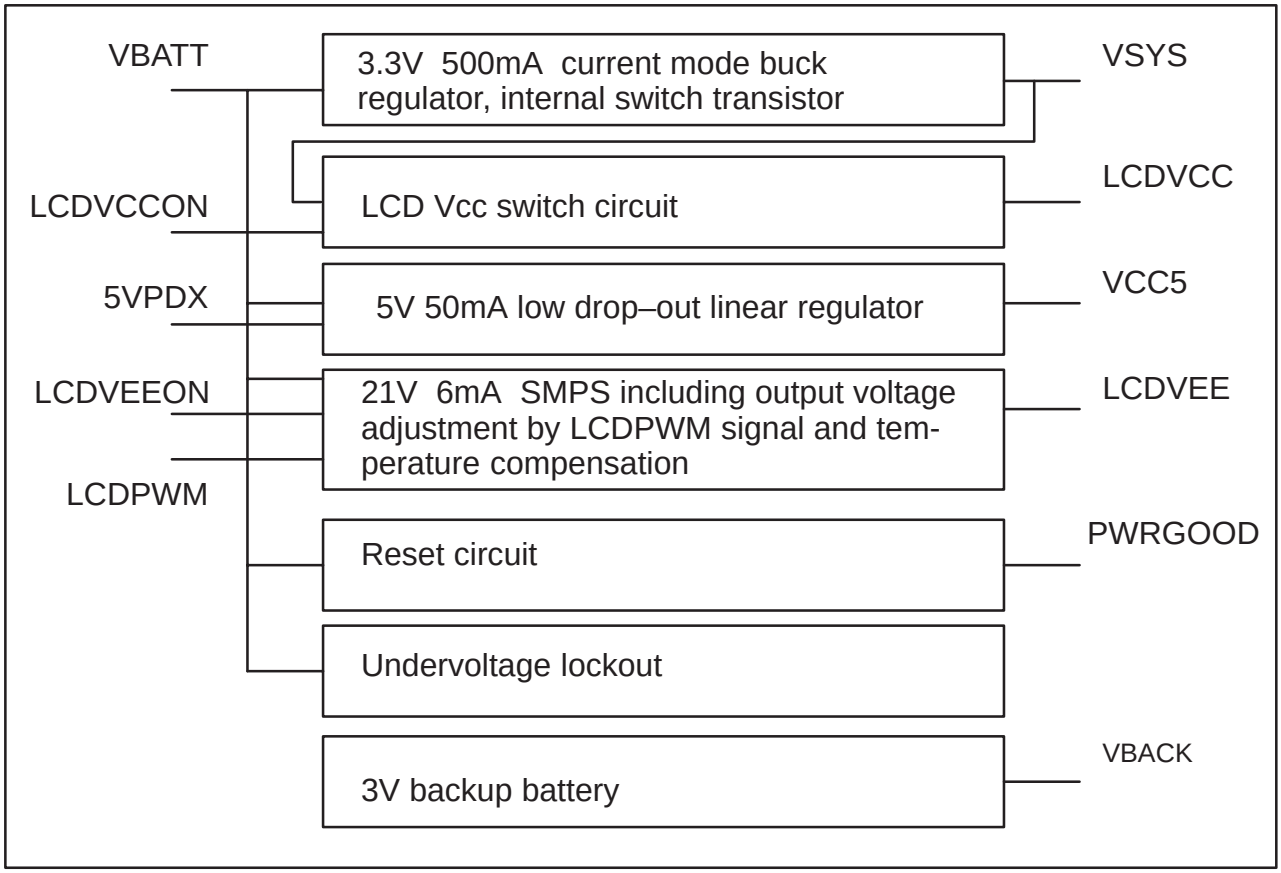

Figure 9. PDAPWRU block diagram

Table 23. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
LCDVCCON	LCD Vcc on/off	PROCU
LCDVEEON	LCD Vee on/off	PROCU
LCDPWM	PWM signal for LCD voltage control	PROCU
5VPDX	5V regulator powerdown	PROCU
VB	Battery voltage	B2B / VB

Note 1. B2B = Board to board connector between PDA and CMT modules

Table 24. External Signals and Connections, Outputs

Signal Name	Signal description	To (1)
VSYS	System voltage 3.3V	PROCU, SIRU
VCC5	5V for FLASH and RBUS	PROCU
PWRGOOD	Reset signal for CPU	PROCU
VBACK	Backup battery voltage to RTC	PROCU
LCDVCC	LCD Vcc to LCDM	LCMCON / LCDVCC
LCDVEE	LCD Vee to LCDM	LCMCON / LCDVEE

Note 1. LCMCON = LCD module connector on PDA module

Table 25. Electrical characteristics

Parameter	Mini-mum	Typi-cal	Max-mum	Units	Notes/conditions
Input voltage range of VB	5.0		11.0V	V	maximum no–harm voltage of VB line
Battery voltage VB	5.0	7.2	8.8	V	max voltage is during charge pulses with cycled battery
VSYS shut-down	4.9	5.0	5.1	V	VB for shutdown operation
	5.9	6.0	6.1	V	VB for cancel of shutdown
VSYS	3.135	3.3	3.465	V	tolerance over temperature and load range
		100	450	mA	output current, regulator I_{max}=500mA
		85		%	efficiency at I_{out}=200mA VB=6.0V
		82		%	efficiency at I_{out}=200mA VB=8.0V
		68		%	efficiency at I_{out}=10mA VB=8.2V
		86		%	efficiency at I_{out}=10mA VB=5.5V
	25	40	100	mV	output voltage ripple
		1.4	3	mA	supply current, no load connected
	159	200	212.5	kHz	oscillator frequency
LCDVEE	18	22	25	V	depending on temperature, typical value at room temperature
	1.3	2	3.5	mA	output current, regulator I_{max}=6mA
		75		%	efficiency at I_{out}=2mA VB=7.2V
			250	mV	output voltage ripple
		0.78		mA	supply current, no load
		330		kHz	operation frequency

Table 25. Electrical characteristics (continued)

Parameter	Mini-mum	Typi-cal	Max-mum	Units	Notes/conditions
VCC5	4.825	5.0	5.175	V	tolerance over temperature and load range
		120	225	mV	dropout voltage at I=50mA
		30		mA	regulator I_{max}=50mA peak current 100mA
		0.4	1.2	mA	ground pin current (supply current)
PWRGOOD	3.04	3.08	3.11	V	reset threshold at room temperature
	140	240	560	ms	power–on reset pulse width
		30		ppm/C	reset threshold temperature coefficient
VBACK	2.5	3.0	3.2	V	
		7		µA	nominal load when used
		130		mAh	capacity, charging not possible
Operating tem-perature range	–25		+85	°C	some circuits tolerate wider temperature range

Functional Description

VSYS regulator

System voltage regulator is current–mode pulse width modulation (PWM) dc–dc step–down converter. It has internal switch transistor and current sense resistor for current–mode control. Oscillator makes the switch transistor to turn on at fixed frequency. Switch transistor on time is determined by load taken at output. Current mode feedback makes transient response fast and provides cycle by cycle current limiting. This means that outer loop determines threshold voltage for current sense amplifier to reach to turn switch transistor off. Inner current feedback loop makes response to load current changes fast.

Outer feedback loop takes output voltage information and compares it to reference and drives the error towards zero in order to keep regulation. This kind of control keeps good regulation at output in rapidly changing load conditions. Tradeoff is high operation current in very light loads because oscillator is running all the time.

VSYS regulator operates at discontinuous conduction mode (DCM) at light loads. This means that current through inductor decreases to zero before new switch transistor turn–on pulse comes and current through inductor starts to increase. At heavy loads inductor current does not go to zero and operation is in continuous conduction mode (CCM).

The controller has internal 1.23V bandgap reference and soft start circuitry for power–up. Overcurrent comparator disconnects the controller in short circuit conditions. After this soft start cycle is made in power–up. Output ripple voltage is determined by output capacitor ESR value which is minimized to reduce EMI. Shutdown mode is used when battery voltage decreases down to 5V to prevent battery from overdischarge. In shutdown all circuits are in lowest power state.

LCDVEE regulator

LCD bias voltage is made by step–up dc–dc controller. Control scheme is current limited pulse frequency modulation (PFM). External switch transistor and current sense resistor are required. Maximum inductor current goes through current sense resistor. Because required regulator output current is small (3mA), resistor value is selected so that current through inductor is low to reduce EMI. Also switch transistor ON–resistance need not be lowest possible. Pulse frequency control is made without oscillator, maximum on–time and minimum off–time are used in pulse control. When output voltage is out of regulation the switch turns on and it stays on until maximum on–time turns it off or inductor current reaches its maximum value set by current sense resistor. When the switch turns off, minimum off–time is waited.

After this the switch stays off until output voltage drops out of regulation. This control results current pulses which are delivered on load demand and 'skipped' when in regulation, 'pulse skipping' regulation. Benefits are very low supply current at light loads because of no oscillator and high energy conversion efficiency. Because pulses come at unspecified time intervals switching noise is in broad frequency range. However maximum inductor current is set to lowest practical value and output capacitor ESR is selected for low value to reduce EMI.

Output voltage is adjusted by LCDPWM signal from PROCU. This pulse width modulated signal is first converted to analog dc voltage by RC–filter. This signal is fed to regulator feedback pin through a resistor which determines the scale at which the LCD display bias voltage can be adjusted. Temperature compensation for bias voltage is made by resistor divider connected to regulator feedback pin. Bias voltage is controlled by two NTC resistors so that optimum LCD contrast bias voltage is followed accurately by the regulator in temperature range between –20°C and +65°C. Because feedback pin comparator voltage is 1.5V and regulator output voltage is over 20V high accuracy feedback resistors are needed for fairly accurate output voltage.

Shutdown is controlled by PROCU. Because this is boost regulator there is current path from input to output which must be cut separately in shutdown. Control switch is placed between regulator output and load.

VCC5 regulator

5V output is used only for data writing to FLASH memory and RBUS signals. Regulator is taken out of shutdown when it is needed. This simple linear regulator has pnp control transistor and overcurrent/overtemperature protection circuitry. Maximum current is 50mA. Peak current is 100mA. At higher loads case heats up and regulator is shut off for very short time and restarted to check if high load remains. If so thermal cycling results. Typical turn–on time for the regulator is 50µs. Only small output capacitor is needed as external component. However, its ESR value must be within certain limits depending on capacitance and load current in order to get stable regulator output.

Reset circuit

Purpose of the reset circuit is to generate proper reset to the CPU and also disable CPU operation when Vsys is below CPU Vcc range. When the battery is plugged in reset circuit generates proper reset pulse when Vsys is risen up to CPU Vcc range. Threshold difference between ”power good” and ”power not good” is about 0.02V.

Undervoltage lockout (UVLO)

Battery voltage is compared to accurate reference diode to detect too low battery voltage. Below this HW limit comparator shuts down VSYS regulator to prevent battery from overdischarge. There is higher SW limit for PDA but VSYS regulator current drains the battery when left unused for long period. After UVLO there is only reference diode and two comparators taking current from battery. UVLO has hysteresis and is cancelled when battery voltage is risen to 6.0V. Only way to do this is by charging or plugging in fresh battery. Hysteresis is made to avoid unsuccessful power–ups. When lockout voltage level is reached battery voltage rises because load is removed.

Input filter

LC–lowpass filter is used between battery and regulators. EMI is not big problem in regulator outputs but EMI conducted from switchmode regulator inputs to battery line needs filtering. Also attenuation of EMI from CMT devices in battery line to PDA regulators is welcomed. Good ground planes and placement of PDA power block to metal cavity and low output ripple voltages keep radiated EMI at low level.

Backup battery

Real time clock is kept running by backup battery only when main battery is not connected. At nominal RTC load 130mAh capacity of backup battery gives over two years of RTC operation when main battery is not connected. Backup battery is not chargeable.

Main components

- 3.3V current mode PWM controller IC
    - MAX763AESA from Maxim
- 5V linear regulator
    - LP29801M5–5.0 from National Semiconductor
- 21V switch mode PFM controller IC
    - MAX772ESA from Maxim
- PWRGOOD reset circuit
    - MAX809T from Maxim
- 3.0V primary back–up battery, 130mAh
    - CR2320 with custom made pins from Matsushita

SIRU

Introduction

IrDA transceiver and RS232 buffer are located to this module. Infrared interface conforms to the Infrared Data Association Serial Interface (SIR) Physical Layer LInk Specification.

SIRU functions:
– external interface signalling (IrDA and RS232)

Technical Description

Table 26. External Signals and Connections, Inputs

Signal Name	Signal description	From (1)
VSYS	System voltage 3.3V	PDAPWRU
TXD	External serial data from 9000	SC / SYSTXD
RSTXD	Serial data from PROCU module	PROCU
RSENX	RS buffer enable	PROCU
RSSHDX	RS buffer shutdown	PROCU
IRSHD	IR tranceiver shutdown	PROCU

Note 1. SC = System Connector

Table 27. External Signals and Connections, Outputs

Signal Name	Signal description	To (1)
RXD	External serial data to 9000	SC / SYSRXD
RSRXD	Serial data to PDA module	PROCU

Note 1. SC = System Connector

Main components

– IR tranceiver
  – Temic IrDA SIR integrated transceiver TFDS3000
  – Shutdown pin
– RS 232 buffer
  – MAX3222CAP transceiver from Maxim
  – Two transmitters, two receivers
  – Generates EIA/TIA–232 compatible signal levels

[This page intentionally left blank]